HIGH SPEED COMPARATOR FOR A SAR CONVERTER WITH RESISTOR LOADING AND RESISTOR BIAS TO CONTROL COMMON MODE BIAS

ABSTRACT OF THE DISCLOSURE

High speed comparator for a SAR converter with resistor loading and resistor bias to control common mode bias. A differential comparator having positive and negative inputs and positive and negative outputs is disclosed. The comparator includes a current source for driving current from a supply to a common node. A differential pair of transistors is disposed such that one side of the source/drain paths are tied together and to the common node, with the other side of the source/drain paths thereof for each of the transistors in the differential pair interfaced to the positive and negative outputs, respectively for applying drive thereto. A first resistor load is disposed between the positive output and a supply reference opposite in polarity to the supply. A second resistor is disposed between the negative output and the supply reference. The gate of the one of the transistors in the pair associated with the positive output is connected to the negative input and the gate of the other of the transistors in the pair is connected to the positive input. The current through the current source defines the common mode bias. A ratiometric bias circuit having associated therewith a bias resistor with a current driven there through is provided that controls the current through the current source, such that it is a ratio of the current through the bias resistor.